Abstract

Consistent with an example embodiment, the amount of time required for testing circuits that contain a plurality of different clock domains is reduced. According to the embodiment, during selection of the input test pattern to test logic circuits between a timing sensitive flip-flop in a first clock domain that captures a response that depends on test data in a source flip-flop in a second, different clock domain, account is taken of whether the data in the first flip-flop will change value if it is clocked when the response is captured. If not, it may be assumed that uncertainty about the timing relationship of different clock domains does not introduce uncertainty with respect to the data from the timing sensitive flip-flop, so that the response data at the second flip-flop can be treated as reliable.